LISTING OF THE CLAIMS:

1. (Withdrawn) A method of forming an integrated semiconductor structure comprising the steps of:

providing a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

fabricating at least one PFET and at least one NFET on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

2. (Withdrawn) The method of Claim 1 wherein said at least one PFET and at least one NFET are formed by the steps of: forming a gate dielectric on a surface of the semiconductor substrate; forming patterned gate conductors on the gate dielectric; blocking some of the patterned gate conductors with a block mask; forming source/drain regions in the unblocked areas; removing the block mask; forming another block mask over areas containing the source and drain regions; and forming source/drain regions in the previously unblocked areas.

3. (Withdrawn) The method of Claim 2 further comprising forming spacers on exposed sidewalls of each patterned gate conductor prior to said blocking step.

4. (Withdrawn) The method of Claim 2 wherein said gate dielectric is formed by a thermal process or deposition.

5. (Withdrawn) The method of Claim 2 wherein the patterned gate conductors are formed by deposition and etching.

6. (Withdrawn) The method of Claim 1 wherein the at least one NFET comprises source/drain regions formed by ion implanting a dopant selected from the group consisting of arsenic and phosphorus into the semiconductor substrate.

7. (Withdrawn) The method of Claim 1 wherein the at least one PFET comprising source/drain regions formed by ion implanting a dopant selected from the group consisting of boron and antimony into the semiconductor substrate.

8. (Withdrawn) The method of Claim 1 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

9. (Withdrawn) The method of Claim 1 wherein said fabricating comprises placing the at least one PFET such that the current flow of the at least one PFET is pointed to the notch.

10. (Withdrawn) The method of Claim 1 wherein said fabricating comprises placing the at least one NFET such that the current flow of the at least one NFET is perpendicular to the notch.

11. (Currently amended) An integrated semiconductor structure comprising

a semiconductor substrate comprising a Group IV semiconducting material that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

at least one PFET and at least one NFET located on the semiconductor substrate, said at least one PFET and said at least one NFET each having a device channel parallel to a surface of said semiconducting substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction.

12. (Currently amended) The integrated semiconductor structure of Claim 11 wherein said Group IV semiconducting material is ~~semiconductor structure is a semiconducting material~~ selected from the group consisting of Si, SiGe, SiC, and SiGeC~~, GaAs, InAs, InP and other like III/V compound semiconductors~~.

13. (Currently amended) The integrated semiconductor structure of Claim 12 wherein ~~the semiconductor material~~ said Group IV semiconducting material is Si.

14. (Original) The integrated semiconductor structure of Claim 11 wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.

15. (Original) The integrated semiconductor structure of Claim 14 wherein the gate dielectric is an oxide.

16. (Original) The integrated semiconductor structure of Claim 14 wherein the patterned gate conductor comprises polySi.

17. (Original) The integrated semiconductor structure of Claim 11 wherein the at least one PFET and the at least one NFET each include source/drain regions, wherein the source/drain regions of the at least one PFET lie perpendicular to the source/drains of the at least one NFET.

18. (Newly added) An integrated semiconductor structure comprising

a semiconductor substrate that has a (110) surface orientation and a notch pointing in a <001> direction of current flow; and

at least one PFET and at least one NFET located on the semiconductor substrate, wherein said at least one PFET has a current flow in a <110> direction and the at least one NFET has a current flow in a <100> direction, said <110> direction is perpendicular to the <100> direction, wherein the at least one NFET and the at least one PFET each comprise a gate dielectric located on the semiconductor substrate, a patterned gate conductor located on portions of the gate dielectric, and spacers located on exposed sidewalls of the patterned gate conductor.